CLAIMS

We claim:

1. *A logic gate comprising:*

a first pull-down device having a first input line coupled thereto;

a second pull-down device having a second input line coupled thereto;

a first pull-up device having an input to be driven by an output of the second pull-down device;

a second pull-up device having an input to be driven by an output of the first pull-down device; and

a keeper coupled to at least one of the first pull-down device and the second pull-down device.

2. The logic gate of Claim 1, wherein the keeper comprises:

a first n-type metal oxide semiconductor transistor having a drain coupled to the output of the first pull-down device and a gate to be driven by the output of the second pull-down device; and

a second n-type metal oxide semiconductor transistor having a drain coupled to the output of the second pull-down device and a gate to be driven by the output of the first pull-down device.

3. The logic gate of Claim 1, wherein the keeper comprises:

a first p-type metal oxide semiconductor transistor having a drain coupled to the first input line and a gate to be driven by the second input line; and

a second p-type metal oxide semiconductor transistor having a drain coupled to the second input line and a gate to be driven by the first input line.

4. A domino logic circuit comprising:

a plurality of dynamic logic gates; and

a plurality of static logic gates coupled to the dynamic logic gates such that the dynamic gates and the static gates are alternately connected in series, the static logic gates each comprising

a first pull-down device having a first input line coupled thereto;

a second pull-down device having a second input line coupled thereto;

a first pull-up device having an input to be driven by an output of the second pull-down device; and

a second pull-up device having an input to be driven by an output of the first pull-down device; and

a keeper coupled to at least one of the first pull-down device and the second pull-down device.

5. The domino logic circuit of Claim 4, wherein the keeper comprises:

a first n-type metal oxide semiconductor transistor having a drain coupled to the output of the first pull-down device and a gate to be driven by the output of the second pull-down device; and

a second n-type metal oxide semiconductor transistor having a drain coupled to the output of the second pull-down device and a gate to be driven by the output of the first pull-down device.

6. The domino logic circuit of Claim 4, wherein the keeper comprises:

a first p-type metal oxide semiconductor transistor having a drain coupled to the first input line and a gate to be driven by the second input line; and

a second p-type metal oxide semiconductor transistor having a drain coupled to the second input line and a gate to be driven by the first input line.